

APS-01-002B

IAW

May 21, 2004



To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/826,752 04/16/04 |
| Romeo Emmanuel J. Alvarez |
| METHOD FOR FORMING A WAFER LEVEL |
| CHIP SCALE PACKAGE, AND PACKAGE |
FORMED THEREBY

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on May 24, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Step B. Ackerman 5/24/04

APS-01-002B


U.S. Patent 6,072,236 to Akram et al., "Micromachined Chip Scale Package," discloses a wafer level process utilizing micromachining to fabricated chip scale packages.

U.S. Patent 6,468,892 to Baker et al., "Front Side Coating for Bump Devices," describes a method utilizing a solder mask at the wafer level for forming bumps on chip scale packages.

U.S. Patent Application Publication US 2002/0027257 A1 to Kinsman et al., "Method for Fabricating a Chip Scale Package Using Wafer Level Processing and Devices Resulting Therefrom," describes a method for fabricating a chip scale package utilizing wafer level processing.

U.S. Patent 6,578,754 to Tung, "Pillar Connections for Semiconductor Chips and Method of Manufacture," discusses pillar-shaped connections from a semiconductor chip to a substrate and method for making the connections.

Sincerely,

A handwritten signature in black ink, appearing to read "Stephen B. Ackerman", with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

